In the Specification:

Please replace paragraph [0010] on page 3 with the following rewritten paragraph:

[0010] The sequencers control the application of the operations in accordance with the timing characteristics of their respective memory modules. For example, each of the sequencers controls the application speed of the sequence of operations in accordance with the access speed of the respective memory module. A single sequencer may control the application of the test algorithms to a plurality of memory modules that operate on a common clock domain. Consequently, logic for controlling application timing and sequencing of the test pattern domain is incorporated within the sequencers, and need not be distributed within the individual memory modules or maintained by the BIST controller.

Please replace paragraph [0072] on page 16 with the following rewritten paragraph:

[0072] FIG. 9D is an example data structure of parameters 68 for the SET ADDRESS command. For this command, parameters 68 includes an ~~and~~ address field (ADDRESS) that sets a specific memory address for application of a BIST step. This may be useful in conjunction with the SINGLE WORD ACCESS command. Parameters 68 also include a limit (LIMIT) field for specifying a maximum address limit for the test algorithm. In one embodiment, the LIMIT field comprises a 2-bit data field for setting the limit to: (1) the maximum address of the largest of the memory modules 12 of the device block 6, (2) the maximum address divided by two, (3) the maximum address divided by four, and (4) the maximum address divided by eight.

Please replace paragraph [0073] on page 16 with the following rewritten paragraph:

[0073] FIG. 9E is an example data structure of parameters 68 for the SINGLE WORD ACCESS command. For this command, parameters 68 include ~~includes~~ an enable address change (ENADC) bit that controls whether the receiving sequencers 8 should change their respective current BIST addresses after applying the step. If enabled, the address increment / decrement (ADD INC/DEC) bit controls whether the current BIST address should be incremented or decremented. The invert bits (IB) field, invert row (IR), and invert column (IC) fields can be used to specify data patterns for testing memory modules 12, such as solid, checkerboard, horizontal and vertical stripes data patterns, as described above in reference to the EXECUTE command.

The data field (DATA) is used to supply a default value for input data for read operations of the tested memory modules 12.

Please replace paragraph [0075] on page 17 with the following rewritten paragraph:

[0075] Table 3 illustrates an example "Blanket March" BIST algorithm stored and issued by BIST controller 4 in accordance with the described command protocol. As illustrated, this memory test algorithm can be described in as few as six commands using the command protocol. Each of the commands directs the receiving sequencers 8 to issue ~~issues~~ sequences of memory operations that traverse the entire memory space in a defined direction. Moreover, several of the commands direct the sequencers to apply multiple memory operations to each address within the available memory space. In this manner, complex BIST algorithms can be easily distributed throughout and applied by the constituent components of the hierarchical self-test architecture.

Please replace paragraph [0079] on page 18 with the following rewritten paragraph:

[0079] In turn, each receiving memory interface 10 translates the data and address signals based on the physical characteristics of each respective memory module 12 (92, 94), and applies the translated signals to the memory modules (96). In addition, for read memory accesses (97), memory interfaces 10 automatically compare ~~compares~~ the data read from the respective memory modules 12 with the expected data (98). Based on the comparison, memory interfaces 10 update respective BIST failure signals to report the status of the tested memory module 12 (100).